REMARKS

Claim 26 has been rejected on new grounds, namely as allegedly being unpatentable over Van Hook (U.S. Patent No. 5,812,147) in view of Gostin (U.S. Patent No. 5,832,290), which was not necessitated by Applicants' amendment of claim 26. In the prior office action response mailed 06/26/2006, claim 26 was rewritten in independent form and was otherwise the same claim 26 that was originally filed. Accordingly, Applicants respectfully request that the finality of the present office action be withdrawn and that the present office action be changed to a non-final office action.

The Examiner argues: "Note that the new grounds rejection for claims 26, 27, 29, 30, 31 and 32 were necessitated by the amendments. The limitations of claim 26 were required to be rejected in order to reject claims 31 and 32."

In response, Applicants assert that the Examiner could have argued the rejection of claims 31 and 32 as allegedly unpatentable over Van Hook in view of Gostin, including the limitations of claim 26, without specifically rejecting claim 26 as allegedly unpatentable over Van Hook in view of Gostin. Thus, although the limitations of claim 26 were required to be rejected in order to reject claims 31 and 32 as allegedly unpatentable over Van Hook in view of Gostin, claim 26 was not itself required to be rejected as allegedly unpatentable over Van Hook in view of Gostin in order to reject claims 31 and 32. Therefore, Applicants reiterate that the rejection of claim 26 as allegedly unpatentable over Van Hook in view of Gostin was not necessitated by Applicants' amendment of claim 26. Accordingly, Applicants respectfully request that the finality of the present office action be withdrawn and that the present office action be changed to a non-final office action.

Applicant note that claim 11 has been rewritten in independent form and is otherwise the same claim 11 that the Examiner examined in the present office action mailed 02/09/2007. Applicants respectfully request that the Examiner focus particular attention on Applicants' argument for claim 11, because Applicants respectfully believe that Applicants' argument for the patentability of claim 11 over the cited prior art is highly persuasive and that claim 11 is accordingly allowable over the cited prior art.

The Examiner objected to the title, stating: "The title is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed... Examiner suggests amending the current title back to the original title. Examiner withdraws the objection to the original title." In response, Applicants have amended the current title back to the original title.

The Examiner objected to claim 26, stating: "Claim 26 objected to because of the following informalities: line 3 of claim26 is written, "providing the processor" and would perhaps be better written as "providing a processor" to avoid any issues with regard to antecedent basis... Appropriate correction is required." In response, Applicants have amended claim 26 in accordance with the preceding suggestion by the Examiner.

The Examiner rejected claims 1-4, 8, 18, 20 and 22-24 under 35 U.S.C. § 102(b) as allegedly being anticipated by Van Hook (U.S. Patent No. 5,812,147).

The Examiner rejected claims 26, 27 and 30 under 35 U.S.C. § 102(b) as allegedly being anticipated by Access and Alignment of Data in an Array Processor (herein Lawrie).

The Examiner rejected claims 5-7, 9-14, 16, 17, 19, 26, 27 and 29-32 under 35 U.S.C. §

103(a) as allegedly being unpatentable over Van Hook (U.S. Patent No. 5,812,147) in view of Gostin (U.S. Patent No. 5,832,290).

The Examiner rejected claims 21 and 28 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Van Hook in view of AMD 64-bit Technology (herein AMD).

The Examiner rejected claims 28 and 29 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Lawrie in view of AMD 64-bit Technology (herein AMD).

Applicants respectfully traverse the title objection, § 102 and § 103 rejections with the following arguments.

35 U.S.C. § 102(b): Claims 1-4, 8, 18, 20 and 22-24 (Van Hook)

The Examiner rejected claims 1-4, 8, 18, 20 and 22-24 under 35 U.S.C. § 102(b) as allegedly being anticipated by Van Hook (U.S. Patent No. 5,812,147).

Since claims 2-3, 8, 20, and 24 have been canceled, the rejection of claims 2-3, 8, 20, and 24 under 35 U.S.C. § 102(b) is moot.

Applicants respectfully contend that Van Hook does not anticipate claim 1, because Van Hook does not teach each and every feature of claim 1. For example, Van Hook does not teach the feature: "wherein the data elements of each subcolumn are stored in different vector register files".

The Examiner's analysis is based on the following assumption by the Examiner regarding Van Hook: "Note that registers in a particular column are considered to be a register file". The Examiner's analysis of the FIG. 2A of Van Hook, as allegedly supported in Van Hook, col. 4, lines 51-55, includes the following components: (1) N=32 and each of the N rows is a vector register having 128 bits; (2) M = 4 and each column is a vertical array of 32 words, each word having 32 bits and encompassing two successive slices (s0-s1, s2-s3, s44-s5, or s6-s7) of the vector register in which each such word is located; (3) K=8 and each column consists of 8 subcolumns, each subcolumn consisting of 4 words, the 4 words appearing in 4 consecutive rows.

Thus the Examiner's analysis requires that in FIG. 2A of Van Hook, the data elements of each subcolumn are stored in a same column and thus in a same vector register file, and not in different vector register files as is required by claim 1.

In contrast, Applicants direct the Examiner's attention to FIGS. 1 and 2 of Applicants'

patent application. For example, the subcolumn elements R0[0], R1[0], R2[0], R3[0] of the subcolumn 128 is addressed in FIG. 1 as register R128. In FIG. 2, said subcolumn elements R0[0], R1[0], R2[0], R3[0] are shown in the registers Y0[0], Y1[1], Y2[2], Y3[3] of the different vector register files V0, V1, V2, V3, respectively.

Based on the preceding arguments, Applicants respectfully maintain that Van Hook does not anticipate claim 1, and that claim 1 is in condition for allowance. Since claims 4, 18, and 22-23 depend from claim 1, Applicants contend that claims 4, 18, and 22-23 are likewise in condition for allowance.

35 U.S.C. § 102(b): Claims 26, 27 and 30 (Lawrie)

The Examiner rejected claims 26, 27 and 30 under 35 U.S.C. § 102(b) as allegedly being anticipated by Access and Alignment of Data in an Array Processor (herein Lawrie).

Applicants respectfully contend that Lawrie does not anticipate claim 26, because Lawrie does not teach each and every feature of claim 26.

As an example of why Lawrie does not anticipate claim 26, Lawrie does not teach the feature: "M≥2" and "executing an instruction by said processor, said instruction performing an operation on a first array of the set of arrays, said operation being performed with selectivity with respect to the data elements of the first array; and providing M multiplexors respectively coupled to the M vector register, wherein the values associated with the M multiplexors control said selectivity".

The Examiner argues: "Lawrie discloses the processor of claims 18 and 25, wherein the processor further comprises M multiplexors respectively coupled to the M vector register files, and wherein the values associated with the M multiplexors control said selectivity (page 100 col 1 second paragraph).... Note that, according to Wordnet ® 2.0 © 2003 Princeton University, a multiplexor is "a device that can interleave two or more activities"; therefore, the mechanism used to choose what values are put into the register file, a mechanism that must exist in this invention, is considered to include a multiplexor for each element."

In response, Applicants respectfully contend that the Examiner has not alleged that Lawrie explicitly teaches the preceding feature of claim 26. Instead, the Examiner appears to be arguing that Lawrie inherently teaches the preceding feature of claim 26. In response, Applicants respectfully contend that the preceding inherency argument by the Examiner does not conform to

the legal test for inherency.

Under case law, the alleged inherency must **necessarily and inevitably** follow from the teachings in the prior art and a high probability of occurrence is not sufficient demonstrating inherency. See MPEP 2112(IV) which recites: "The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) (reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art); *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is **necessarily** present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' " *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)... "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy,* 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original)" (bold emphasis added).

As applied to claim 26, Applicants assert that it does not necessarily and inevitably follow from the teachings in Lawrie coupled with the Examiner's cited definition of "multiplexor" that M multiplexors are respectively coupled to the M vector registers subject to $M \geq 2$.

First, a mechanism that determines the values to be put in a register file is not necessarily

a device that interleaves two or more values. For example, an operation of copying a fixed array of values into a register file does not necessarily require utilization of a device that interleaves two or more values.

Second, even if it is inherent to have a device that interleaves two or more values in order to determine the values to be put in a register file (which it is not as explained *supra*), it is not inherent that M multiplexors are respectively coupled to the M vector registers such that $M \geq 2$. For example using the Examiner's definition of "multiplexor", a single multiplexor (i.e., one device that interleaves two or more values) could be used to put values in M register files such that $M \geq 2$. Thus, it does not necessarily and inevitably follow from the teachings in Lawrie that M multiplexors must be used to put values in M register files subject to $M \geq 2$.

Moreover, it does not necessarily and inevitably follow from the teachings in Lawrie that the values associated with M multiplexors must be used to control the claimed selectivity, since the selectivity can be controlled by either a single multiplexor or by a variety of other logic devices.

Based on the preceding arguments, Applicants respectfully maintain that Lawrie does not anticipate claim 26, and that claim 26 is in condition for allowance. Since claims 23-25 and 30 depend from claim 26, Applicants contend that claims 27 and 30 are likewise in condition for allowance.

35 U.S.C. § 103(a): Claims 5-7, 9-14, 16, 17, 19, 26, 27, 29-32 (Van Hook in view of Gostin)

The Examiner rejected claims 5-7, 9-14, 16, 17, 19, 26, 27, and 29-32 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Van Hook (U.S. Patent No. 5,812,147) in view of Gostin (U.S. Patent No. 5,832,290).

Claims 5-7 and 19

Since claims 5-7 and 19 depend from claim 1, which Applicants have argued *supra* to not be unpatentable over Van Hook under 35 U.S.C. §102(b), Applicants maintain that claims 5-7 and 19 are likewise not unpatentable over Van Hook in view of Gostin under 35 U.S.C. §103(a).

In addition with respect to claims 5-7, Van Hook in view of Gostin does not disclose the feature: "M≥2" and "wherein the processor further comprises M multiplexors respectively coupled to the M vector register files".

The Examiner argues: "Gostin discloses a vector register file controlled by a multiplexer (col 5 lines 1-5)."

In response, Applicants disagree with the Examiner's interpretation of Gostin, col. 5, lines 1-5. The "vector register file 102" referred to in Gostin comprises multiple vector register files as defined by the Examiner in reference to Van Hook, as indicated in the following description of the "vector register file 102" in Gostin, col. 4, line 64 - col. 5, line 1: "vector register file 102 comprises four banks each having 512 64-bit registers (elements) partitioned into four vector registers of 128 registers each, with each bank coupled to three read ports and one write port." Gostin, col. 5, lines 1-5 is ambiguous as to how many multiplexors are within the

vector register file 102. Thus for M vector register files within the vector register file 102 such that $M \geq 2$, Gostin, col. 5, lines 1-5 does not teach or suggest precisely M multiplexors respectively coupled to the M vector register files, as required by claim 5-7.

In addition with respect to claims 5-7, Van Hook in view of Gostin does not disclose the feature: "wherein each multiplexor of the M multiplexors comprises a set of binary switches subject to each binary switch being on or off and respectively represented by a binary bit 1 or 0 such that the value of the multiplexor consists of the composite value of said binary bits".

The Examiner has not provided a citation to either Van Hook or Gostin that allegedly teaches or suggests the preceding feature of claims 5-7.

In addition with respect to claims 5-6, Van Hook in view of Gostin does not disclose the feature: "wherein the M multiplexors are adapted to respond to a command to read a subcolumn of the matrix by reading the data elements of the subcolumn from the M vector register files to the subcolumn of the matrix in accordance with a read-subcolumn mapping algorithm" (claim 5); and "wherein the M multiplexors are adapted to respond to a command to write a subcolumn of the matrix by mapping the data elements of the subcolumn to the M vector register files in accordance with a write-subcolumn mapping algorithm" (claim 6).

The Examiner argues that Van Hook discloses the preceding features of claims 5-6, aside from the multiplexors being hardware multiplexors.

Applicants assert that a read-subcolumn mapping algorithm and a write-subcolumn mapping algorithm is enabled only if a subcolumn, as defined in claim 1 from which claims 5-6

depend, is delineated with respect to the location of the subcolumn within its respective column.(including the length of the subcolumn or its equivalent). Van Hook does not teach or suggest such subcolumns and their identification within their respective columns. Although Van Hook teaches that every element within a column can be addressed, Van Hook does not teach defining a subcolumn, which requires a specification of two numbers (e.g., the starting location of the subcolumn and the ending location of the subcolumn). Therefore, a read-subcolumn mapping algorithm and a write-subcolumn mapping algorithm is not enabled in Van Hook.

Claims 9-14 and 16-17

Since claims 9-10 have been canceled, the rejection of claims 9-10 under 35 U.S.C. § 103(a) is moot.

Applicant note that claim 11 has been rewritten in independent form and is otherwise the same claim that the Examiner examined in the present office action mailed 02/09/2007.

Applicants respectfully contend that claim 11 is not unpatentable over Van Hook in view of Gostin, because Van Hook in view of Gostin does not teach or suggest each and every feature of claim 11. For example, Van Hook in view of Gostin does not teach or suggest the features: "said M vector register files collectively storing a matrix of L data elements, ... wherein the data elements of each subcolumn are stored in different vector register files".

The Examiner does not set forth any argument directed specifically to claim 11, but appears to view the argument that the Examiner made with respect to claim 3 as likewise applying to claim 11, because the Examiner states in item 8 on page 5 of the office action: "Regarding claims 4, Van Hook discloses the processor of claims 3 and 11, wherein the data

elements of each subcolumn are adapted to be stored in different relative register locations of the different vector register files, and wherein the data elements of each row are adapted to be stored in a same relative register location of the different vector register files (col 2 lines 23-26)... ***See claims 3 and 11***" (emphasis added).

In response, Applicants respectfully contend that the argument that the Examiner made with respect to claim 3 does not apply to claim 11 for the following reason. Claim 3 recited: " said M vector register files **adapted to collectively store** a matrix of L data elements, ... wherein the data elements of each subcolumn **are adapted to be stored** in different vector register files" (emphasis added), which is an intended use. Thus, the Examiner's argument for claim 3 ("*Note that, as with most any register file, there are no limitations to rearranging the information stored in memory. Using storing and load instructions, any set of information can be stored in a plurality of different configurations within the register file*") is persuasive.

In contrast, claim 11 recites "said M vector register files **collectively storing** a matrix of L data elements, ... wherein the data elements of each subcolumn **are stored** in different vector register files" (emphasis added), which is not an intended use but is instead a limitation that Van Hook must teach or suggest in order to support the alleged unpatentability of claim 11 over Van Hook in view of Gostin.

Applicants respectfully contend that Van Hook does not teach or suggest the preceding feature of claim 11. Applicants note that the Examiner's analysis is based on the following assumption by the Examiner regarding Van Hook: "Note that registers in a particular column are considered to be a register file". The Examiner's analysis of the FIG. 2A of Van Hook, as allegedly supported in Van Hook, col. 4, lines 51-55, includes the following components: (1)

N=32 and each of the N rows is a vector register having 128 bits; (2) M = 4 and each column is a vertical array of 32 words, each word having 32 bits and encompassing two successive slices (s0-s1, s2-s3, s44-s5, or s6-s7) of the vector register in which each such word is located; (3) K=8 and each column consists of 8 subcolumns, each subcolumn consisting of 4 word, the 4 words appearing in 4 consecutive rows.

Thus the Examiner's analysis requires that in FIG. 2A of Van Hook, the data elements of each subcolumn are stored in a same column and thus in a same vector register file, and not in different vector register files as is required by claim 11.

In contrast, Applicants direct the Examiner's attention to FIGS. 1 and 2 of Applicants' patent application. For example, the subcolumn elements R0[0], R1[0], R2[0], R3[0] of the subcolumn 128 is addressed in FIG. 1 as register R128. In FIG. 2, said subcolumn elements R0[0], R1[0], R2[0], R3[0] are shown in the registers Y0[0], Y1[1], Y2[2], Y3[3] of the different vector register files V0, V1, V2, V3, respectively.

Based on the preceding arguments, Applicants respectfully maintain that claim 11 is not unpatentable over Van Hook in view of Gostin, and that claim 11 is in condition for allowance. Since claims 12-14 and 16-17 depend from claim 11, Applicants contend that claims 12-14 and 16-17 are likewise in condition for allowance.

In addition with respect to claims 13-14, Van Hook in view of Gostin does not disclose the feature: "M≥2" and "wherein the method further comprises providing M multiplexors respectively coupled to the M vector register files".

The Examiner argues: "Gostin discloses a vector register file controlled by a multiplexer

(col 5 lines 1-5)."

In response, Applicants disagree with the Examiner's interpretation of Gostin, col. 5, lines 1-5. The "vector register file 102" referred to in Gostin comprises multiple vector register files as defined by the Examiner in reference to Van Hook, as indicated in the following description of the "vector register file 102" in Gostin, col. 4, line 64 - col. 5, line 1: "vector register file 102 comprises four banks each having 512 64-bit registers (elements) partitioned into four vector registers of 128 registers each, with each bank coupled to three read ports and one write port." Gostin, col. 5, lines 1-5 is ambiguous as to how many multiplexors are within the vector register file 102. Thus for M vector register files within the vector register file 102 such that $M \geq 2$, Gostin, col. 5, lines 1-5 does not teach or suggest precisely M multiplexors respectively coupled to the M vector register files, as required by claim 13-14.

In addition with respect to claims 13-14, Van Hook in view of Gostin does not disclose the feature: "wherein each multiplexor of the M multiplexors comprises a set of binary switches subject to each binary switch being on or off and respectively represented by a binary bit 1 or 0 such that the value of the multiplexor consists of the composite value of said binary bits".

The Examiner has not provided a citation to either Van Hook or Gostin that teaches or suggests the preceding feature of claims 13-14.

In addition with respect to claims 13-14, Van Hook in view of Gostin does not disclose the feature: "the M multiplexors are adapted to respond to a command to read a subcolumn of the matrix by reading the data elements of the subcolumn from the M vector register files to the

subcolumn of the matrix in accordance with a read-subcolumn mapping algorithm" (claim 5); and "wherein the M multiplexors are adapted to respond to a command to write a subcolumn of the matrix by mapping the data elements of the subcolumn to the M vector register files in accordance with a write-subcolumn mapping algorithm" (claim 6).

The Examiner argues that Van Hook discloses the preceding features of claims 13-14, aside from the multiplexors being hardware multiplexors.

Applicants assert that a read-subcolumn mapping algorithm and a write-subcolumn mapping algorithm is enabled only if a subcolumn, as defined in claim 1 from which claims 13-14 depend, be delineated with respect to the location of the subcolumn within its respective column.. However, Van Hook does not teach or suggest such subcolumns and their identification within their respective columns. Therefore, a read-subcolumn mapping algorithm and a write-subcolumn mapping algorithm is not enabled in Van Hook.

Claims 26-27 and 29-32

Applicants respectfully contend that claim 26 is not unpatentable over Van Hook in view of Gostin, because Van Hook in view of Gostin does not teach or suggest each and every feature of claim 26. For example, Van Hook in view of Gostin does not teach or suggest the feature: "$M \geq 2$" and "providing M multiplexors respectively coupled to the M vector register files".

The Examiner argues: "Van Hook discloses the limitations of claims 26: Van Hook discloses a method for processing matrix data comprising: ... Executing an instruction by said processor, said instruction performing an operation on a first array of the set of arrays, said operation being performed with selectivity with respect to data elements of the first array (col 2

lines 24-28); and ... Providing M multiplexers respectively coupled to the M vector register files, wherein the values associated with the M multiplexers control said selectivity (see claim 5)."

With respect to the preceding feature in relationship to claim 5, the Examiner argues: "Gostin discloses a vector register file controlled by a multiplexer (col 5 lines 1-5)."

In response, Applicants disagree with the Examiner's interpretation of Gostin, col. 5, lines 1-5. The "vector register file 102" referred to in Gostin comprises multiple vector register files as defined by the Examiner in reference to Van Hook, as indicated in the following description of the "vector register file 102" in Gostin, col. 4, line 64 - col. 5, line 1: "vector register file 102 comprises four banks each having 512 64-bit registers (elements) partitioned into four vector registers of 128 registers each, with each bank coupled to three read ports and one write port." Gostin, col. 5, lines 1-5 is ambiguous as to how many multiplexors are within the vector register file 102. Thus for M vector register files within the vector register file 102 such that $M \geq 2$, Gostin, col. 5, lines 1-5 does not teach or suggest precisely M multiplexors respectively coupled to the M vector register files, as required by claim 26.

In further response, claim 5 does not recite the feature: "executing an instruction by said processor, said instruction performing an operation on a first array of the set of arrays, said operation being performed with selectivity with respect to the data elements of the first array; ... wherein the values associated with the M multiplexors control said selectivity." Therefore, the Examiner's arguments are not applicable to the preceding feature of claim 5 and the Examiner has not offered any argument to support the Examiner's contention that Van Hook in view of Gostin teaches or suggests the preceding feature of claim 26. Accordingly, Applicants assert that the Examiner has not established a *prima facie* case of obviousness in relation to claim 26.

Based on the preceding arguments, Applicants respectfully maintain that claim 26 is not unpatentable over Van Hook in view of Gostin, and that claim 26 is in condition for allowance. Since claims 27 and 29-32 depend from claim 26, Applicants contend that claims 27 and 29-32 are likewise in condition for allowance.

In addition with respect to claim 29, Van Hook in view of Gostin does not disclose the feature: "wherein said performing an operation includes rearranging the data elements of the first array within the first array.'

The Examiner argues that the Examiner's argument made with respect to claim 22 applies likewise to claim 29.

In response, Applicants respectfully contend that the argument that the Examiner made with respect to claim 22 does not apply to claim 29 for the following reason. Claim 22 recites: "wherein the instruction is **adapted to rearrange** the data elements of the first array within the first array" (emphasis added), which is an intended use. Thus, the Examiner's argument for claim 22 ("*Examiner asserts that a vector register file, like the one disclosed in Van Hook, is clearly able to rearrange its data*") is persuasive.

In contrast, claim 29 recites "wherein said performing an operation includes **rearranging** the data elements of the first array within the first array" (emphasis added), which is not an intended use but is instead a limitation that Van Hook must teach or suggest in order to support the alleged unpatentability of claim 29 over Van Hook in view of Gostin.

Applicants respectfully contend that Van Hook does not teach or suggest the preceding feature of claim 29, and the Examiner has not provided any evidence allegedly demonstrating

that Van Hook teaches or suggests the preceding feature of claim 29.

In addition with respect to claim 32, Van Hook in view of Gostin does not disclose the feature: "wherein each multiplexor of the M multiplexors comprises a set of binary switches subject to each binary switch being on or off and respectively represented by a binary bit 1 or 0 such that the value of the multiplexor consists of the composite value of said binary bits."

The Examiner argues that the Examiner's argument made with respect to claim 5 applies likewise to claim 32.

In response, Applicants rely on Applicants' arguments presented *supra* in relation to claim 5 as likewise applying to claim 32.

35 U.S.C. § 103(a): Claims 21 and 28 (Van Hook in view of AMD)

The Examiner rejected claims 21 and 28 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Van Hook in view of AMD 64-bit Technology (herein AMD).

Since claims 21 depends from claim 1, which Applicants have argued *supra* to not be unpatentable over Van Hook under 35 U.S.C. §102(b), Applicants maintain that claim 21 is likewise not unpatentable over Van Hook in view of AMD under 35 U.S.C. §103(a).

Since claim 28 depends from claim 26, which Applicants have argued *supra* to not be unpatentable over Van Hook under 35 U.S.C. §102(b), Applicants maintain that claim 28 is likewise not unpatentable over Van Hook in view of AMD under 35 U.S.C. §103(a).

In addition with respect to claims 21 and 28, Applicants respectfully contend that the Examiner's argument for modifying Van Hook with the alleged teaching of AMD is not persuasive.

The Examiner argues: "It would have been obvious at the time of the invention for one of ordinary skill in the art to allow the processing system of Van Hook to include vector-move and vector-shift instructions in order to have instructions that "insert an exact copy of the first array into the second array" and "rearrange the data elements of the first array within the first array", respectively."

In response, Applicants assert that the alleged motivation to modify Van Hook ("instruction that " **insert** an exact copy of the first array into the second array"") teaches away from what is recited in claims 21 and 28 ("wherein the instruction **does not insert** an exact copy of the first array into the second array").

Therefore, Applicants respectfully contend that the Examiner has not established a *prima facie* case of obviousness in relation to claims 21 and 28.

35 U.S.C. § 103(a): Claims 28 and 29 (Lawrie in view of AMD)

The Examiner rejected claims 28 and 29 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Lawrie in view of AMD 64-bit Technology (herein AMD).

Since claims 28 and 29 depend from claim 26, which Applicants have argued *supra* to not be unpatentable over Lawrie under 35 U.S.C. §102(b), Applicants maintain that claims 28 and 29 are likewise not unpatentable over Lawrie in view of AMD under 35 U.S.C. §103(a).

In addition with respect to claim 28, Applicants respectfully contend that the Examiner's argument for modifying Lawrie with the alleged teaching of AMD is not persuasive.

The Examiner argues: "It would have been obvious at the time of the invention for one of ordinary skill in the art to allow the processing system of Lawrie to include vector-move and vector-shift instructions in order to have instructions that "insert an exact copy of the first array into the second array" and "rearrange the data elements of the first array within the first array", respectively."

In response, Applicants assert that the alleged motivation to modify Lawrie ("instruction that " **insert** an exact copy of the first array into the second array"") teaches away from what is recited in claim 28 ("wherein said copying **does not insert** an exact copy of the first array into the second array").

Therefore, Applicants respectfully contend that the Examiner has not established a *prima facie* case of obviousness in relation to claim 28.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0457.

Date: 03/26/2007

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